in-481

16K × 8 MICROPROCESSOR COMPATIBLE MEMORY SYSTEM

The in-481 is a 16K x 8 Random Access Memory that utilizes the Intel 2107B 4K Dynamic RAM chip. The memory and all refresh and control circuitry are on one PC board. The in-481 is expandable to a maximum of 64K x 8 by the use of four memory cards. The in-481 card is designed to interface directly with the IMM8-82 and the IMM8-83 CPU cards. Since the characteristics of these two cards are governed by either the 8008 or the 8080 microprocessors, it is also possible to use the in-481 with any CPU using these devices. The physical size of the in-481 is the same as the IMM Series. The address, data I/O, and power pin-outs are the same as the IMM6-28.

Applications*

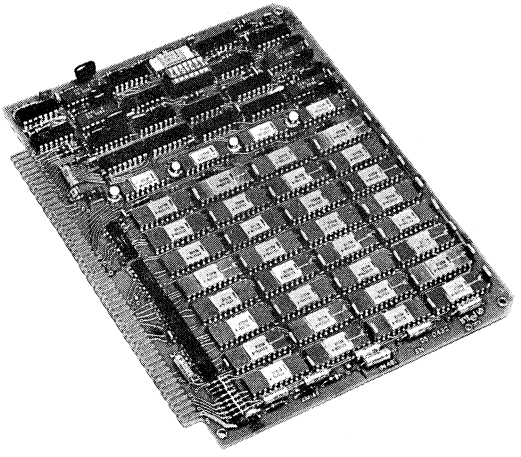
8008

When using the in-481 in an 8008 or 8008-1 microprocessor based system, the access and cycle times are such that WAIT states need not be entered. All refresh, write and read cycle requests are synchronized to specific CPU states and requests. This means that the in-481 is totally transparent to the CPU. During normal CPU operation all refreshing is done during the T_1 state of the 8008; during a HALT or HOLD state the memory refresh is synchronized to the ϕ_1 clock and occurs every 7.5 μsec. It should be noted, that a power-up reset circuit initializes all control circuitry on the in-481.

8080

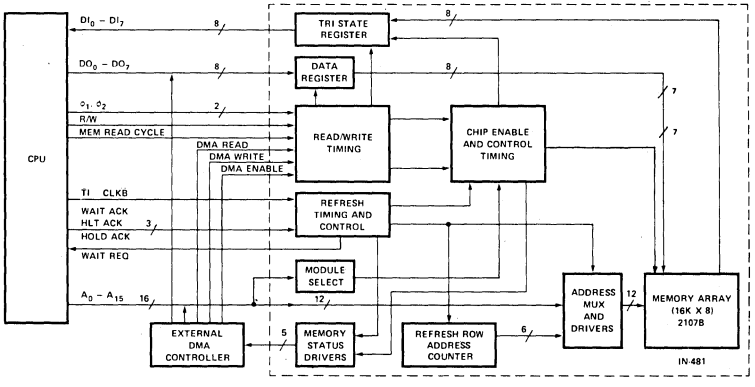
When using the in-481 in an 8080 microprocessor based system, the memory components used are faster in both cycle and access times in order to minimize the total number of WAIT cycle requests. All refresh, read and write cycle requests are again synchronized to specific CPU states or requests. Because of the 2.0 μsec instruction cycle time of the 8080, a single WAIT state or a possible double WAIT state is required during memory refresh. A memory refresh is initiated once every 31 μsec and it is synchronized to the positive edge of SYNC during the T_1 state. Normally a single WAIT state between T_2 and T_3 states is required if the memory is in the

*While the in-481 and in-481-1 are designed to work with the IMM8-82 and IMM8-83, they are not intended for use in the INTELLEC 8/MOD8 or INTELLEC 8/MOD80 since the current requirements of the in-481 and in-481-1 exceed the 60mA capacity of the INTELLEC +12V power supply.



in-481 FEATURES:

- IMM8-82 and IMM8-83 Compatible
- Automatic Refresh
- Modular Expandability
- Module Interchangeability
- Very High Density
- Board Select
- On Board 4K Address Select
- On Board 4K Enable/Disable
- Input and Output Data Registers
- Low Standby Power



Applications (Continued)

process of performing a read operation. If, however, a write cycle had been initiated during T_3 of the previous subcycle a double WAIT state is requested by the in-481. During the HOLD and HALT states, the refresh requests are synchronized to the ϕ_1 clock and they occur with a period of 25 μsec. It should be noted again that the power-up reset circuit initializes all control circuitry.

DMA

A DMA option is made possible in both 8008 and 8080 systems by means of the HOLD features. The HOLD ACK signal in both the IMM8-82 and IMM8-83 frees the control lines of the in-481 and the in-481-1. This signal is also used by the in-481 to disable the MEM READ CYCLE control input thereby enabling DMA control of the memory. Since refresh is synchronized to the ϕ_1 clock, and since additional state lines are brought out from the in-481, an access control circuit can be implemented to perform DMA. After completion of DMA, the HOLD and WAIT requests to the CPU card are disabled, and memory operation proceds as normal.

SPECIFICATIONS

Dimensions:

8.00 inches x 6.18 inches with 0.5 inch mounting centers.

Capacity:

16K x 8 expandable to 64K x 8 by use of four memory cards

Cycle Time:

in-481	1100 nanoseconds
in-481-1	600 nanoseconds

Access Time:

in-481	650 nanoseconds
in-481-1	450 nanoseconds

Power:

+5V	1.0A
+12V	0.9A
−9V*	30mA

* (−9V is zenered to −5V; optional −5VDC at 5mA)

Operational Modes:

Read (NDRO)
Write

Environment:

Temperature:	0°C to +50°C operating ambient −40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating Up to 50,000 feet non-operating

Connector Type:

Amp	1-67878-0
Winchester	HW50D0111
Viking	3VH50/ICN5
Sylvania	7900-0281-X

PIN NO.	8008	8080
1		
2		
3	GND	GND
4	GND	GND
5	WAIT ACK	WAIT ACK
6	TI	CLK 8
7	DMA READ	DMA READ
8	PWR RESET	PWR RESET
9	*WE	*WE
10	NC	φ2
11	MAD 0	MAD 0
12	MAD 1	MAD 1
13	MAD 2	MAD 2
14	MAD 3	MAD 3
15	MAD 4	MAD 4
16	MAD 5	MAD 5
17	MAD 6	MAD 6
18	MAD 7	MAD 7
19	MAD 8	MAD 8
20	MAD 9	MAD 9
21	WAIT REQ	WAIT REQ
22		
23	MDI 0	MDI 0
24	DB 0	DB 0
25	MDI 1	MDI 1
26	DB 1	DB 1
27	MDI 3	MDI 3
28	DB 3	DB 3
29	MDI 2	MDI 2
30	DB 2	DB 2
31	MDI 5	MDI 5
32	DB 5	DB 5
33	MDI 4	MDI 4
34	DB 4	DB 4

PIN NO.	8008	8080
35	MDI 7	MDI 7
36	DB7	DB 7
37	MDI 6	MDI 6
38	DB 6	DB 6
39	SYS ENC	SYS ENC
40		
41	ADD ENA	ADD ENA
42	ADD ENB	ADD ENB
43	−9V	−9V
44	−9V	−9V
45	DMA READ ENABLE	DMA READ ENABLE
46	HOLD ACK	HOLD ACK
47		
48		
49	+12V	+12V
50	+12V	+12V
51		
52		
53		
54		
55		
56		
57		
58		
59	MAD 13	MAD 13
60	MAD 12	MAD 12
61		
62		
63	MA 14	MA 14
64		
65	MAD 15	MAD 15
66	MAD 14	MAD 14
67	DB IN	MEM READ CYC
68	MA 15	MA 15
69		

PIN NO.	8008	8080
70		
71	*READ	*READ
72		
73	HALT ACK	HALT ACK
74	SYNCA	DMA φ2 DISABLE
75		
76		
77		
78		
79		
80		
81		
82		
83		
84		
85	*REF	*REF
86		
87	*BUSY	*BUSY
88	*ENREF	*ENREF
89		
90		
91	GND	GND
92	GND	GND
93		
94	MAD 11	MAD 11
95	R/W	R/W
96	MAD 10	MAD 10
97		
98	φ1	φ1
99	+5	+5
100	+5	+5

*Status signals from in-481.

MEMORY SYSTEMS